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Twisted Pair Control Module User's Guide

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Introduction

Echelon's LONWORKS™ Twisted Pair Control Modules contain the core elements for OEM node designs using LONWORKS technology. The core elements of a Control Module are:

- NEURON® 3150™ CHIP
- Crystal clock circuit
- 32 kbyte JEDEC MO-052 AE PLCC memory socket (32-pin rectangular)
- Transceiver circuit
- Unbuffered access to the NEURON CHIP I/O, ~SERVICE, and ~RESET signals.

The family of LONWORKS Twisted Pair Control Modules includes the TP/XF-78 Control Module (transformer coupled, 78 Kbps), TP/XF-1250 Control Module (transformer coupled, 1.25 Mbps), and TP-RS485 Control Module (EIA standard RS-485, 39 Kbps). All three Control Modules share a common footprint and I/O interface to allow systems with different media requirements to share common application electronics board designs. Designers requiring high levels of noise immunity and isolation will select the TP/XF Control Modules over the lower cost TP-RS485 Control Module.

Audience

The *LONWORKS Twisted Pair Control Module User's Guide* provides specifications and user instruction for customers who have purchased any of Echelon's Twisted Pair Control Modules. These include the TP/XF-1250 Control Modules, TP/XF-78 Control Modules, and TP-RS485 Control Modules.

Content

This manual provides detailed technical specifications on the electrical and mechanical interfaces and operating environment characteristics for the Control Modules.

This document also provides guidelines for migrating applications from a LONBUILDER™ Developer's Workbench Emulator to a Control Module-based product design. Complete references and vendor sources are included to simplify the task of integrating the Control Modules with application electronics.

This document has a list of references in Chapter 8. Whenever a reference document is addressed, a superscript number corresponding to the reference has been placed in the text, i.e., Standler[11]. Whenever a specific chapter or section within a reference has been referred to, the reference is enclosed in brackets and the chapter is addressed by number, i.e., Reference [1], Chapter 8.

Related Documentation

The following Echelon documents are suggested reading:

LONBUILDER User's Guide (078-0001-01A)

NEURON C Programmer's Guide (078-0002-01A)

LONBUILDER Startup and Hardware Guide (078-0003-01A)

LONWORKS Interoperability Guidelines (078-0014-01)

NEURON CHIP Advance Information (005-0018-01)

TP-RS485 Twisted Pair Control Module data sheet

TP/XF-1250 Twisted Pair Control Module data sheet

TP/XF-78 Twisted Pair Control Module data sheet

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Electrical Interface

Twisted Pair Control Modules interface to the node application electronics and to the network through two connectors, P1 and P2, respectively. P1 provides access to the NEURON CHIP I/O ~RESET and ~SERVICE pins, and the power connection for the Control Module (see Chapter 4 for power supply requirements). P2 supports connection to the twisted pair data bus as well as access to the network coupling transformer in the TP/XF Control Modules.

P1 and P2 Connector Terminals

The pinout of the P1 and P2 connector terminals is shown in tables 2.1, 2.2, and 2.3. The I/O pin function names defined in table 2.1 are identical to the terms used in the *NEURON CHIP Advance Information*[1] document which defines the functions and electrical characteristics for those signal names listed in table 2.1. The I/O signals are connected directly to the NEURON 3150 CHIP without buffering.

Table 2.1 18-pin I/O Connector (P1) for Control Modules

Name	Pin #	Function
IO0	2	See the NEURON CHIP Advance Information document.
IO1	4	
IO2	6	
IO3	8	
IO4	10	
IO5	11	
IO6	13	
IO7	15	
IO8	17	
IO9	14	
IO10	16	
~RESET	9	
~SERVICE	18	
+5V	12	power supply input
GND	3, 5, 7	power supply ground
	1	no connection

Table 2.2 6-pin Network Connector (P2) for the TP/XF-78 and TP/XF-1250 Control Modules

Name	Pin #	Function
CTB	1	transformer center tap*
CTA	2	transformer center tap*
Data B	3	network data B signal
Data A	4	network data A signal
	5	no connection
	6	no connection

* CTA and CTB must be shorted together on the application electronics board.

Table 2.3 6-pin Network Connector (P2) for the TP-RS485 Control Module

Name	Pin #	Function
	1	no connection
	2	no connection
Data B	3	network data B signal
Data A	4	network data A signal
	5	no connection
	6	no connection

Control Module pin P1.9 is the NEURON CHIP ~RESET pin. The ~RESET pin on the NEURON CHIP may be driven externally or may be used as an open drain output to provide a reset signal for the application circuit. The details of the recommended circuit and loading on the NEURON CHIP ~RESET pin are described in Reference

[1], Chapter 8. The actual reset circuit implemented on the Control Modules is shown in figure 2.1.

The 68 pF capacitors shown in figure 1 increase the Control Module's immunity to ESD transients. This additional capacitance must be considered when designing circuits using the ~RESET signal as an output.

Note: default = pullup on

The ~SERVICE pin of the NEURON CHIP is accessible directly at P1.18. This pin is used for various network installation and maintenance scenarios. The function of this pin is described in Reference [1], Chapter 8. By default, the internal pullup resistor for the ~SERVICE pin is enabled. Typical applications will use the circuit shown in figure 2.2. The internal pullup may be disabled using a compiler directive `#pragma disable_servpin_pullup` in the application code targeted for the node.

Typical applications do not require debounce conditioning of momentary push buttons attached to the ~SERVICE and ~RESET pins. The software response time associated with these inputs is long enough to effectively provide a software debounce for switches with a contact bounce settling time as long as 20 msec.

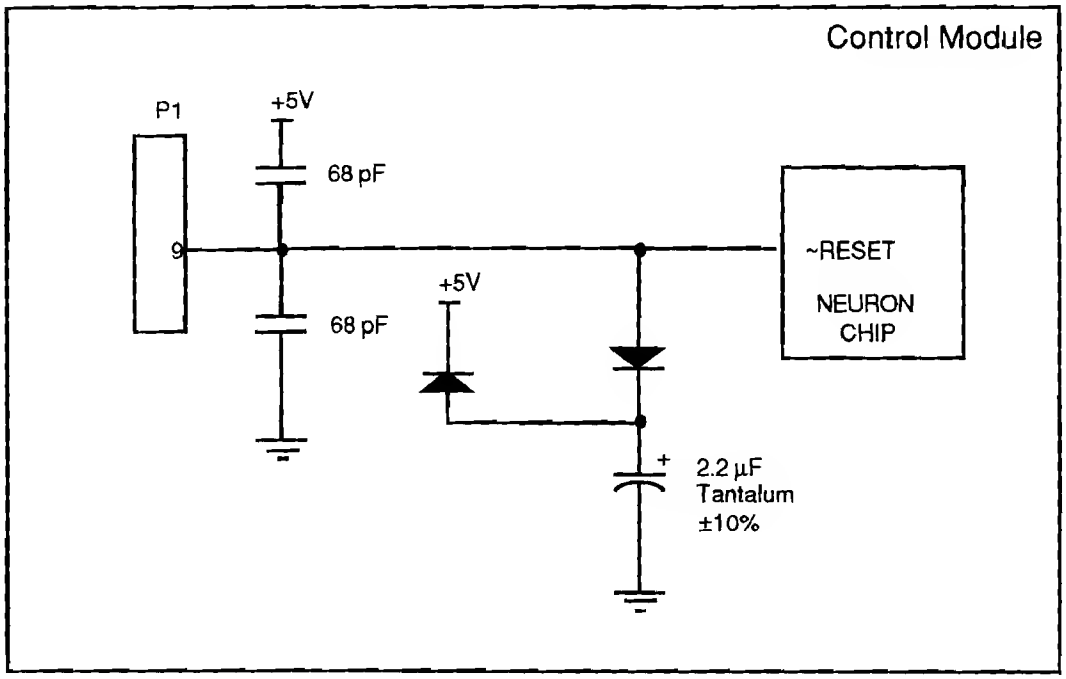


Figure 2.1 Control Module reset circuit

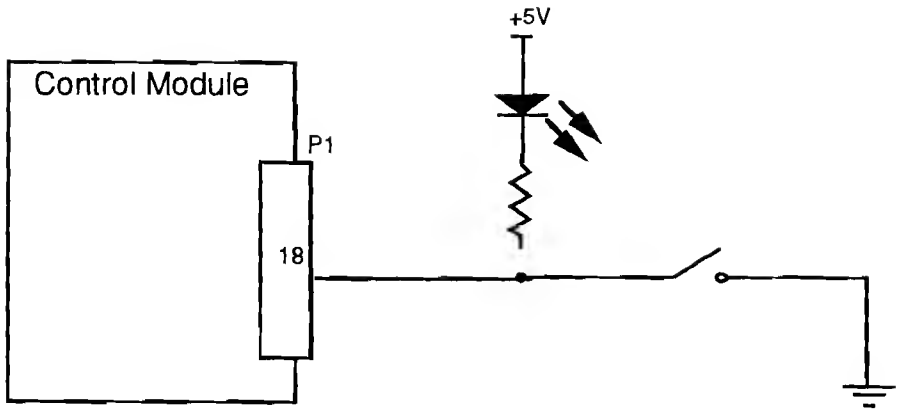


Figure 2.2 Typical ~SERVICE pin circuit

3

Mechanical Considerations

This chapter discusses the mechanical footprint and connectors of the Twisted Pair Control Modules. Details of mounting to an application electronics board are provided.

Mechanical Footprint

The Twisted Pair Control Modules share a common footprint and connectors as shown in figure 3.1. The most common Control Module mounting scenario uses socket strips on the application electronics board which connect with P1 and P2 as shown in figure 3.2. Vendor information for socket strips that mate with the 0.025" (0.64mm) square header posts of P1 and P2 are referenced in table 3.1.

If necessary, taller socket strips may be used to gain more clearance between the Control Module and the application board. Decisions about component placement on the application electronics board must also consider electromagnetic interference (EMI) and electrostatic discharge (ESD) issues discussed in Chapter 6 of this document.

Figure 3.2 also shows the maximum height of parts on both sides of the Control Module. Application designs using the transformer-coupled twisted pair transceivers should maintain a minimum of 0.15" (3.81mm) clearance from P2 pins and traces on the network side of the transformer to achieve the minimum isolation specified for these Modules. Refer to the High Voltage and EMI Keepout sections in Chapter 6 for isolation requirements.

Three plated mounting holes that accept No. 6 (3.5mm) mounting screws are electrically connected to the Control Module ground plane. When the 0.025" (0.64mm) square posts of P1 and P2 are inserted into the sockets they provide enough holding strength (3 oz (85g)/pin) to secure the Control Module against shock and vibration to the operating limits of the components on the Control Module. However, at least one metal standoff and fastening screw located at the mounting hole near the P2 connector is recommended to meet EMI limits and for ESD protection (see Chapter 6).

Figure 3.3 presents the height restrictions of the component side of the Control Module. The board is divided into two height zones: the maximum height of components in the first zone is 0.20" (5.1mm), while the second zone's components are 0.47" (11.9mm). Care should be taken to ensure that no components on the application electronics board interfere with the height restricted areas of the Control Modules.

Figure 3.4 shows the recommended PCB pad layout for the application electronics board to interconnect a Control Module with an application board that has socket strips mounted on the component side.

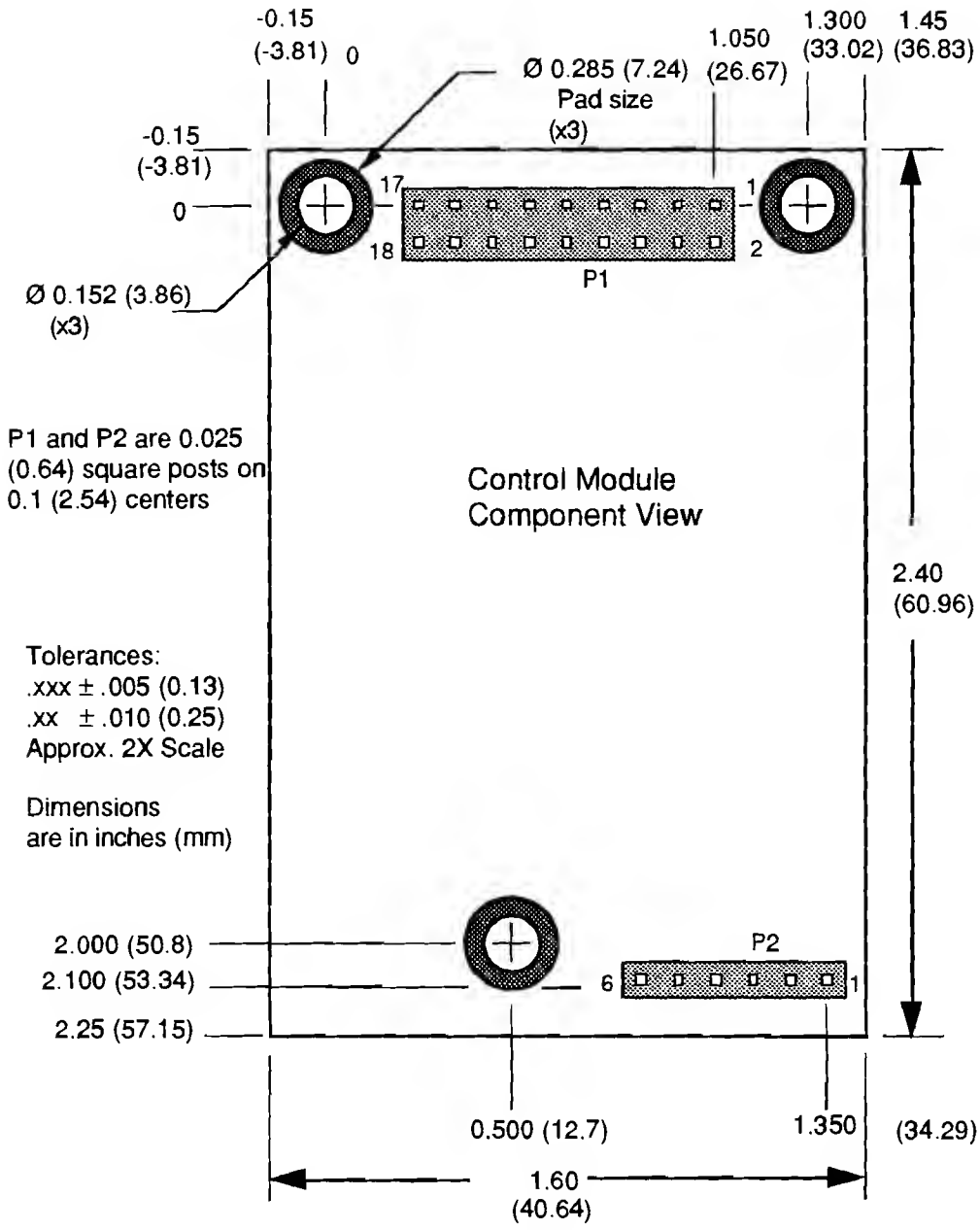
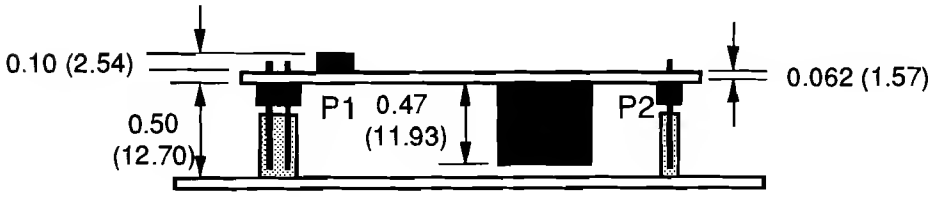


Figure 3.1 Control Module mechanical footprint

Table 3.1 Socket strips suitable for use with the Control Module header pins

Manufacturer	P1: 18-pin (2 X 9)	P2: 6-pin (1 X 6)
Samtec	SSW-109-01-T-D	SSW-106-01-TS
Augat	A015-018-YB-001	A010-006-YB-001
Methode	9000-209-303	9000-106-303



P1 and P2 are 0.025 (0.64)
square posts on 0.1 (2.54) centers

Tolerances:
.xxx ± .005 (0.13)
.xx ± .010 (0.25)
Approx. 1X Scale

Figure 3.2 Recommended spacing between the Control Module and application electronics board.

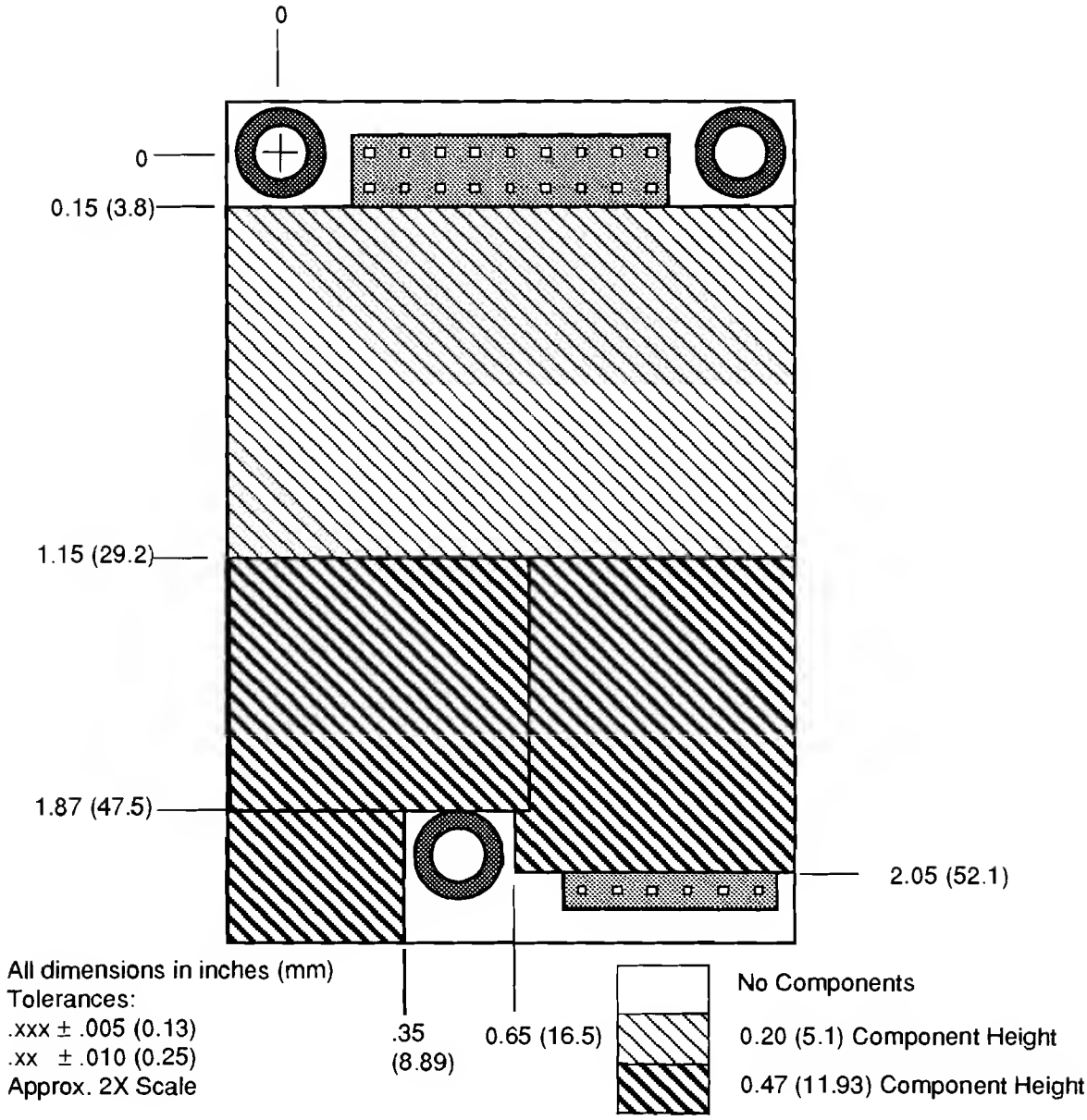
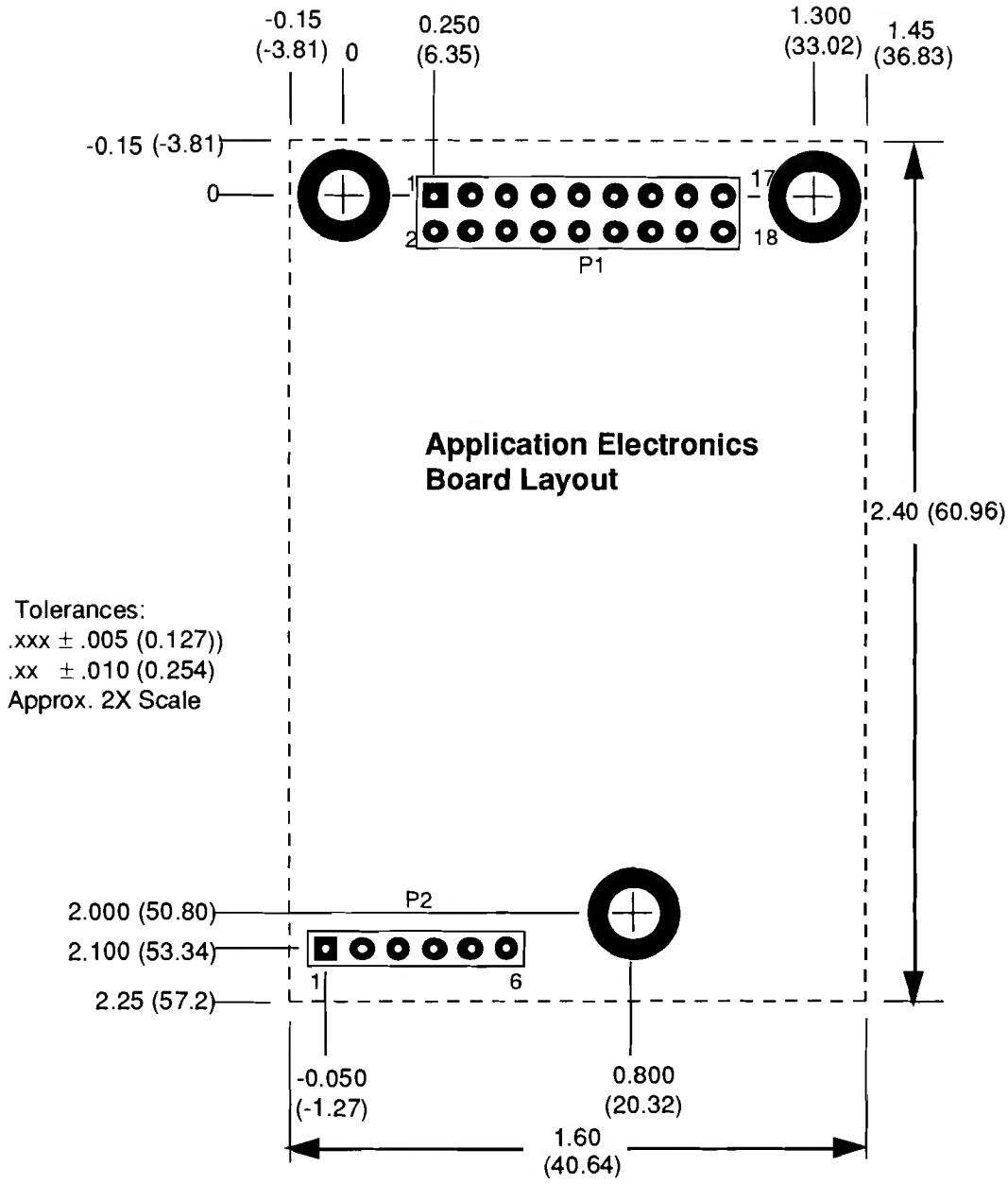


Figure 3.3 Vertical component profile for the Control Modules.



Reference	Pad O.D.	Finished Plated Hole Dia. ±0.003 (0.08)
Mounting	0.285 (7.24)	0.152 (3.86)
P1,P2	0.060 (1.52)	0.035 (0.89)

Figure 3.4 Required pad layout for application electronics board

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Power Requirements

This section describes the power requirements for the Control Modules as well as considerations for noise filtering in order to comply with both conducted and radiated emissions requirements.

Control Module Power Requirements

Twisted Pair Control Modules require a +5V DC power source with sufficient current to power the Control Module in all modes of operation.

The supply current requirements for the Control Modules are outlined in table 4.1, which includes peak requirements for the different operating states of the NEURON CHIP. The Control Modules require a 5V ±5% power supply. The current requirements are characterized for maximum number of nodes on the channel with I/O pins programmed as outputs at a logic low level with no load.

The power supply must ramp to 90% of V_{DD} in less than 30 msec to ensure a clean reset on power-up. This assumes no attached external pullup current on ~RESET. (See Reference [1], Chapter 8)

The values in table 4.1 are subject to change. Please consult current data sheets for the latest information.

Table 4.1 Typical Control Module +5 Volt current requirements

Control Module	**Typical DC Characteristics (+5.0V)**	
	Active, Receive (mA)	Active, Transmit (mA)
TP-RS485 (5 MHz)	30	65
TP/XF-78 (5 MHz)	35	45
TP/XF-1250 (10 MHz)	55	80

Notes:

1. Assumes internal I/O pullups are disabled.
2. Assumes ~SERVICE pullup is enabled.
3. Includes CMOS EPROM running typical application with system code.

Power Supply Decoupling and Filtering

The design for the Control Modules power supply must consider filtering and decoupling requirements of the Control Module. The power supply filter must prevent noise generated by the Control Module and I/O circuit from conducting onto external wires, and in the case of DC-DC switching power supplies, must prevent noise generated by the supply from interfering with module operation. Switching power supply designs must also consider the effects of radiated EMI.

The Control Modules include 2.2µF and 0.1µF power supply bypass capacitors close to pin 12 of P1. In general, a high frequency decoupling capacitor valued at 0.1µF or 0.01µF placed near pin 12 of P1 on the application electronics board is necessary to reduce EMI.

The Control Modules require a clean power supply to prevent RF noise from conducting on to the network through active drive circuits. Power supply noise near the network transmission frequency may degrade network performance.

Attention to the design of the application electronics circuit is also necessary. High-speed signals and inductive loads are common sources of noise which must be managed by separating the logic and I/O power supplies, or by using sufficient filtering and decoupling techniques.

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Network Cabling and Connection

This chapter provides information about cabling and connections for the Twisted Pair Control Modules. This information includes a discussion of wire characteristics, an excerpt from the EIA RS-485 Standard concerning grounding issues, and the bus termination drawing.

Wire Characteristics

The Control Modules are designed for distributed control applications using low-cost twisted pair media. The characteristics of the wire used to implement a network will effect the overall system performance with respect to total distance, stub length, and total number of nodes supported on a single channel. Echelon recommends the use of UL Level IV, 22 AWG twisted pair cable as defined in document: *UL's LAN Cable Certification Program*, Document number 200-120 20M/11/91 (see Reference [16]).

RS-485 Grounding

Proper operation of the transmit and receive circuits requires the presence of a signal return path between the circuit grounds of the equipment at each end of the interconnection. The circuit reference may be established by a third conductor connecting the common leads of devices, or it may be provided by connections in each to an earth reference. Where the circuit reference is provided by a third conductor, the connection between circuit common and the third conductor must contain some resistance (e.g., 100 ohms) to limit circulating current when other ground connections are provided for safety (see Reference [6]).

Bus Termination

It is necessary to terminate the ends of the twisted pair bus to minimize reflections. Failure to terminate the bus will degrade network performance. Figure 5.1 shows the circuit required to terminate a twisted pair bus for the Control Modules.

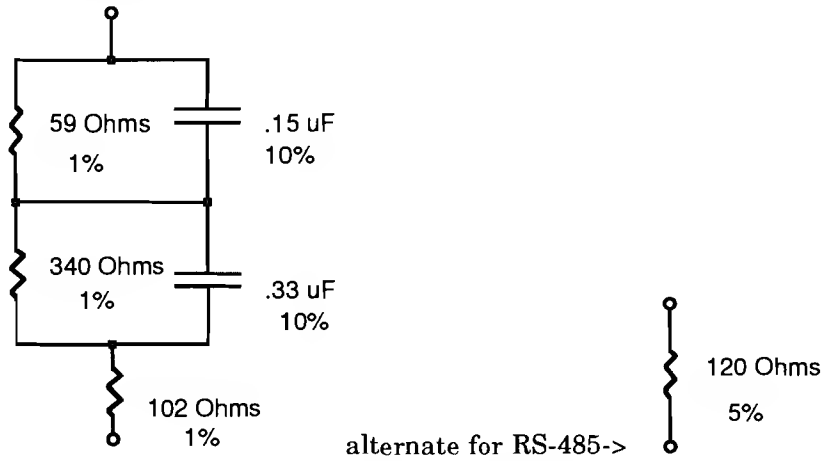

Figure 5.1 Required bus termination for twisted pair networks

6

Design Issues

This chapter looks at design issues. There is a discussion of Electromagnetic Interference (EMI), and Electrostatic Discharge (ESD), and Designing for Interoperability.

EMI Design Issues

The high-speed digital signals associated with microcontroller designs can generate unintentional Electromagnetic Interference (EMI). High-speed voltage changes generate RF currents that can cause radiation from a product if a length of wire or piece of metal can serve as an antenna.

Products that use the Twisted Pair Control Modules will generally need to demonstrate compliance with EMI limits enforced by various regulatory agencies. In the USA, the FCC[7] requires that unintentional radiators comply with Part 15 level "A" for industrial products, and level "B" for products that can be used in residential environments. Similar regulations are imposed in most countries throughout the world[8,9].

Echelon has designed the Twisted Pair Control Modules with low enough RF noise levels for design into level "B" products. Echelon encourages level "B" compliance for all LONWORKS-compatible products. This section describes design considerations for Control Module-based products to meet EMI regulations.

Designing Systems for EMC (Electromagnetic Compatibility)

Echelon has demonstrated that designs using the Control Modules can meet both FCC and VDE level "B" limits. Careful design of application electronics is important to guarantee that a Control Module-based node will achieve the desired EMC. Information on designing products for EMC is available in several forms including books,[10] seminars, and consulting services. This section provides useful design tips for EMC.

EMC Design Tips

- Most of the RF noise originates in the CPU portion of the Control Module, and in any high-frequency or high-speed application circuitry in the node.
- Most of the EMI will be radiated by the network cable and the power cable.
- Filtering is generally necessary to keep RF noise from getting out on the power cable.
- EMI "Keepout" area restrictions should be observed to prevent internal RF noise from coupling onto the network cable.
- The Control Module must be well grounded within the node to ensure that its built-in EMI filtering works properly.

- Early EMI testing of prototypes at a certified outdoor range is an extremely important step in the design of level "B" products. This testing ensures that grounding and enclosure design questions are addressed early enough to avoid most last-minute changes (and their associated schedule delays).

It is possible for a plastic enclosure to be used with Twisted Pair Control Modules in level "B" applications in some specialized configurations. Since external cables must be kept away from the "RF hot" keepout area on the modules (figure 6.1), the product configuration must somehow constrain the routing of cables so that they cannot pass across the surface of the plastic enclosure near the module. During FCC EMI testing, cable position is typically varied to generate maximum emission levels (within constraints of normal product usage).

The three standoff holes on the Control Module are generally not needed for mechanical support, but the hole nearest connector P2 is important for EMI grounding of the Control Module. Best results are achieved by a solid ground connection from the Control Module to the application mother board and to a metalized enclosure using the P2 standoff.

The Twisted Pair Control Modules include adequate filtering on the network data communication lines for most node designs to meet level "B" emission limits. In rare cases, such as designs including circuits with extremely fast edges, additional noise attenuation is required. In such cases it may be necessary to use a common-mode choke, such as muRata's PLT1R53C connected in series with the data communication lines adjacent to the node's external network connector. This choke will provide an additional 10dB-to-15dB of EMI attenuation over the 30-to-500 MHz range. The choke adds a few pF of differential capacitance to the data communication lines, and therefore reduces network performance and may affect intropera bility. In general, application designs should not require a common-mode choke.

Control Module Keepout Areas

Figure 6.1 shows three "keepout" areas on the control modules. Area one, the "EMI Radiated Keepout Area," covers the NEURON CHIP and the PROM. This is the area of the Control Module that generates the most RF noise. Cables, long metal chassis parts, and drive circuits for external cables must be kept away from this part of the Control Module.

Area two, the "EMI Susceptibility Area," is the main twisted pair transceiver area on the Control Module, and any RF energy that couples into this part of the module circuit will be conducted out onto the Local Operating Network cable. High frequency and high-speed circuits should be kept well away from this area of the Control Module (and away from the Local Operating Network connector).

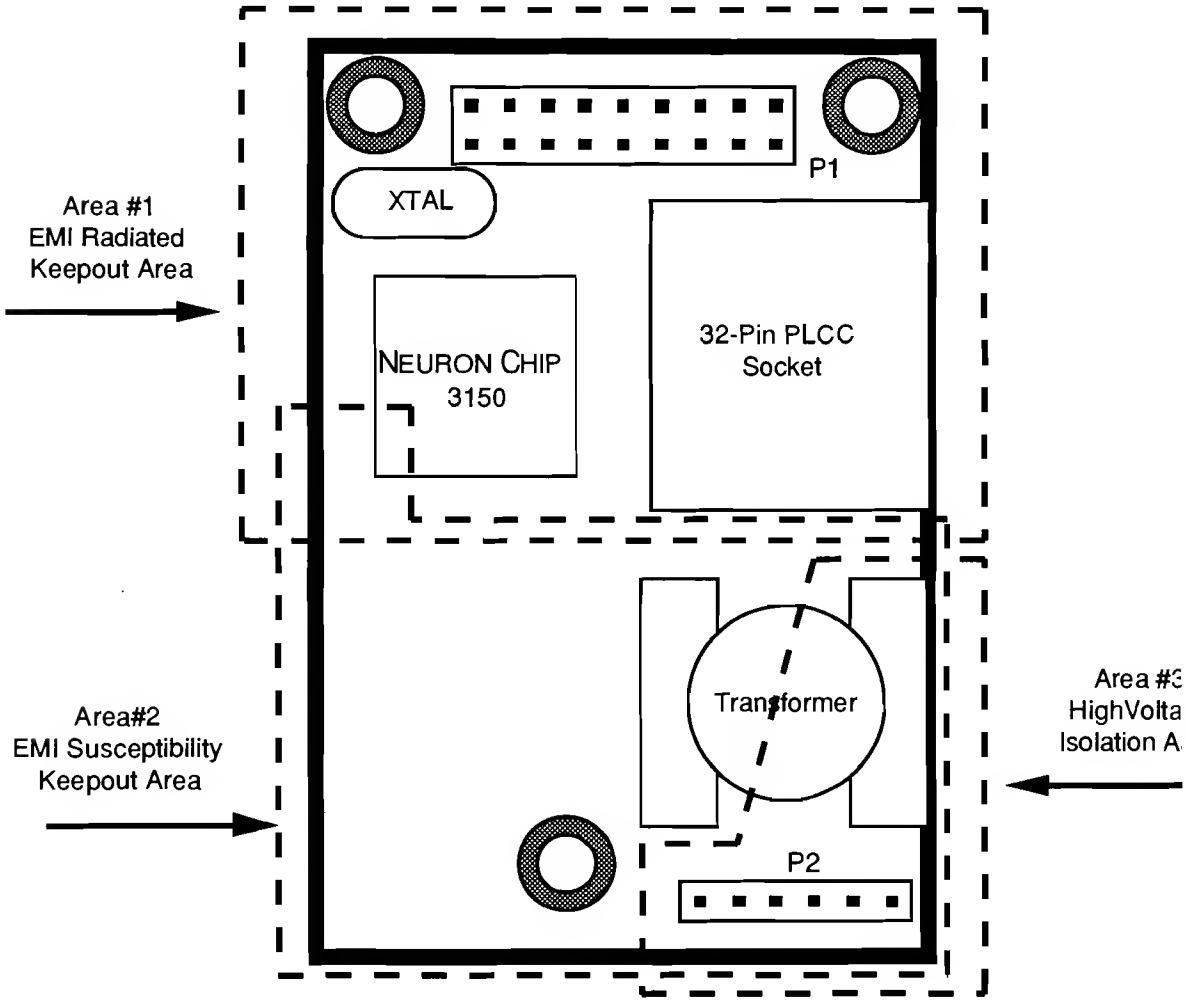

Figure 6.1 Control Module keepout Areas

Area three, which exists on the TP/XF-78 and TP/XF-1250 transformer coupled Control Modules, is the "High Voltage Isolation Area." The transceiver coupling

transformer on these Control Modules provides electrical isolation between the Control Module's local ground (primary side) and the network wiring (secondary side). The transformers and associated filter components are designed to withstand moderately large primary-to-secondary voltages (see the Control Module data sheets for the exact ratings). To take advantage of this isolation, it is important to keep application circuitry, logic ground, metal chassis parts, and other primary-side components at least 0.15 inches (3.8mm) away from the secondary area on the Control Module and the network connector.

ESD Design Issues

Electrostatic Discharge (ESD) is encountered frequently in industrial and commercial use of electronic systems[11]. Reliable system designs must consider the effects of ESD and take steps to protect sensitive components. Static discharges occur frequently in low-humidity environments when operators touch electronic equipment. The static voltages generated by humans can easily exceed 10kV. Keyboards, connectors, and enclosures provide paths for static discharges to reach ESD sensitive components such as the NEURON CHIP. This section describes techniques to design ESD immunity into Control Module-based products.

Designing Systems for ESD Immunity

ESD hardening includes the following techniques:

- Provide adequate creepage and clearance distances to prevent ESD hits from reaching sensitive circuitry;
- Provide low impedance paths for ESD hits to ground;
- Use diode clamps or transient voltage suppression devices for accessible, sensitive circuits

The best protection from ESD damage is circuit inaccessibility. If all circuit components are positioned away from package seams, the static discharges can be prevented from reaching ESD sensitive components. There are two measures of "distance" to consider for inaccessibility: creepage and clearance. Creepage is the shortest distance between two points along the contours of a surface. Clearance is the shortest distance between two points through the air. An ESD hit generally arcs farther along a surface than it will when passing straight through the air. For example, a 20 kV discharge will arc about 0.4 inches (10 mm) through dry air, but the same discharge can travel over 0.8 inches (20mm) along a clean surface. Dirty surfaces can allow arcing over even longer creepage distances.

When ESD hits to circuitry cannot be avoided through creepage, clearance and ground guarding techniques, i.e., at external connector pins, explicit clamping of the exposed lines is required to shunt the ESD current. Consult Standler[11] for advice about ESD and transient protection for exposed circuit lines. In general, exposed lines require diode clamps to the power supply rails or zener clamps to chassis ground in order to shunt the ESD current to ground while clamping the voltage low enough to prevent circuit damage. The NEURON CHIP's I/O and control lines are connected directly to P1 without any ESD protection beyond that provided by the NEURON CHIP itself. If these lines will be exposed to ESD in an application, protection must be added on the application electronics board. Figure 6.2 shows an example of the use of diode clamps to protect the Control Module I/O lines in a keypad scanning application.

The Control Modules use diode clamping (and transformer isolation on the TP/XF-78 and TP/XF-1250 Control Modules) to shunt ESD from the network connector P2 to ground. It is therefore important to provide a low impedance ground path from the mounting hole near P2 to the main system ground.

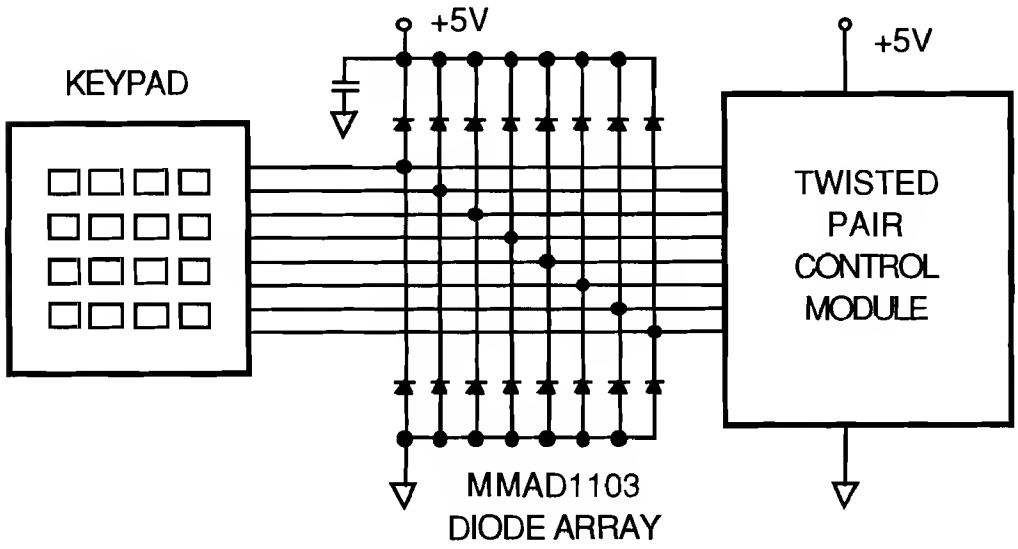

Figure 6.2 Example of diode clamping protection for Control Module I/O lines

Designing for Interoperability

In order to meet minimum input impedance requirements specified in the Echelon interoperability standard regarding 78 kbps and 1.25 Mbps transformer-coupled nodes, the following printed circuit layout guideline for the application electronics board is recommended for use with the TP/XF-78 and TP/XF-1250 Control Modules.

Mutual capacitance of data pair conductors (differential capacitance) from the twisted pair medium tap connector to the connector which mates to the TP/XF Control Module P2 header must be kept within the maximum limit specified in the table below:

Module Type	Maximum mutual data pair conductor capacitance from node's medium tap connector to TP/XF Control Module P2 header
TP/XF-78	5 pF
TP/XF-1250	2 pF

To meet these requirements, PCB trace lengths between the Control Module P2 and the node medium tap connectors should be generally kept less than 5 cm for TP/XF-78 nodes and less than 2 cm for TP/XF-1250 nodes.

7
Programming Considerations

This section explains the integration of Control Modules using the LONBUILDER Developer's Workbench. It covers considerations relating to ROM size specifications, channel definition, target emulation hardware, and PROM specifications.

Application Program Development and Export

Application programs are initially developed, tested, and debugged using the LONBUILDER Developer's Workbench. See the *LONBUILDER User's Guide* for detailed instructions on developing and testing applications. LONBUILDER Emulators with hardware properties set to the values shown in table 7.1 will emulate the functional operation of a Control Module. The backplane network in the LONBUILDER Development Station can also be used to approximate the performance of the twisted pair media used by the Control Modules. To do this, create a `Channel` with `backplane` selected as the transceiver type and use the values shown in table 7.2 for the Bit Rate, Minimum Clock Rate, Average Packet Size, Collision Detect, and Oscillator Accuracy.

The Control Module will support up to 32 Kbytes of 70 ns ROM for storing the system code, application code, and constant data. The NEURON CHIP system image requires the first 16 Kbytes of the ROM, leaving up to 16 Kbytes for application program code and constant data. In the `Hardware Properties` definition, selecting a hardware ROM size of 64 pages (16 Kbytes) will cause the LONBUILDER Developer's Workbench to try to fit the entire application in the NEURON CHIP's internal EEPROM. If the entire application fits in the NEURON CHIP's internal EEPROM, then the application can be changed and downloaded over the network, without burning new PROMs.

Once the application program is fully developed and debugged on an emulator, the application can be exported from the LONBUILDER Developer's Workbench for subsequent programming of a PROM. Again, refer to the *LONBUILDER User's Guide* for detailed instructions on how to do this. Before exporting the application, be sure to change the `HW Type` in the `Target Hardware` display to `Custom`. Also change the `Channel` Definition to the real Control Module transceiver configuration defined in table 7.2. Carefully verify the Channel Definition (Hardware Properties) before doing a Build and Final Export of the image. Improperly specified properties are a common mistake that cause Custom Nodes to appear non-functional.

PROM Considerations

The developer must supply the PROM to contain the exported image. Table 7.3 shows the vendor part numbers for 32 Kbytes, PLCC OTP ROMs that fit the socket on the Control Module. The TP/XF-1250 Control Module has a 10 MHz input clock and therefore requires a 70 ns access time[1]. The standard TP/XF-78 and TP-RS485 Control Modules have a 5 MHz input clock that increases the minimum access to 200ns. Please note that LCC devices that support UV erasures are not physically compatible with the PLCC socket.

Emulation Technology, Inc. sells an adaptor (part number ET 322801K600-YAM) to support programming PLCC devices using standard 600 mil DIP PROM programmers.

LONBUILDER Developer's Workbench, Control Modules, and Custom Nodes

A fully operational Control Module with a PROM containing the system and application program can be attached to a twisted pair network connected to a LONBUILDER Developer's Workbench. See the *LONBUILDER Startup and Hardware Guide* for information on the Evaluation Transceiver Network Connector pinout. See the *LONBUILDER User's Guide* for instructions on how to install and exercise custom nodes on a LONBUILDER Developer's Workbench. If the fully-operational Control Module is being installed on the same LONBUILDER system that was used to program the PROM and the above procedure was followed, the node and channel definitions will already be complete and correct. If the fully-operational Control Module is being installed as a pre-loaded node on a different LONBUILDER system, make sure that the `Hardware Properties` and the `Channel` definition are correctly specified in the LONBUILDER Developer's Workbench before installing the Control Module; tables 7.1 and 7.2 list the correct values to be used for those definitions.

Table 7.1 Hardware properties for Control Modules

HW Property Name	Control_mod	*User's choice*
NEURON CHIP	3150	
Input Clock Rate	5 MHz	*10 MHz for TP/XF-1250*
ROM Size	128 pages	*64 for network downloads*
EEPROM Size	0	
RAM Size	0	

Table 7.2. Channel definition values for Control Modules

Variable	RS-485	78K	1250K
Transceiver Type	Single-ended	Twisted Pair	Twisted Pair
Bit Rate	39.06 Kbps	78.12 Kbps	1250 Kbps
Minimum Clock Rate	5 MHz	5 MHz	10 MHz

Variable (continued)	RS-485	78K	1250K
Number of Priority Slots	0	0	0
Oscillator Accuracy	200 ppm	200 ppm	200 ppm
Average Packet Size	15 bytes	15 bytes	15 bytes
Collision Detect	No & Disabled	No & Disabled	No & Disabled
Bit Sync Threshold	4 bits	N/A	N/A
Layer 1 Time Factors			
Preamble Length	205µS (8 bits)	N/A	N/A
Receive Start Delay	50µS	N/A	N/A
Receive End Delay	0µS	N/A	N/A
Indeterminate Time	100µS	N/A	N/A
Min Interpacket Time	0µS	N/A	N/A
Use Raw Data?	No	N/A	N/A

Table 7.3 Suitable 32-pin JEDEC PLCC, 32 kbyte OTP ROM devices

Supplier	70 ns Access time	150-200 ns Access time
AMD	AM27C256-70JC	AM27C256-200JC
Atmel		AT27C256R-20JC
Catalyst	CAT27HC256N-70	---
Microchip	27HC256-70/L	27C256-20/L
Intel		N27C256-200V10
Signetics		27C256-20A
National		NMC27C256-20
Texas Instruments		TMS27C256-20

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References and Suppliers

This section provides a list of the reference material used in the preparation of this manual. In addition, a list of suppliers for socket strips, ROMS, and the PLCC/DIP adapter is included.

Reference Documentation

[1] NEURON® 3120™ CHIP and NEURON 3150™ CHIP Advance Information, Echelon Systems Corporation, 1991.

[2] Motorola MC143150 NEURON CHIP Data Sheet.

[3] Toshiba TMPN3150 NEURON CHIP Data Sheet.

[4] LONWORKS Custom Node Development Engineering Bulletin, Echelon Corporation, 1992.

[5] Implementing Twisted pair Transceivers with NEURON CHIPS, LONWORKS Engineering Bulletin, Echelon Corporation, March 1992 (preliminary).

[6] EIA RS-485 Standard, Electronic Industries Association, 1983. This document is available through Global Engineering Documents in Irvine, California at (1+714) 261-1455 or (1+800) 854- 7179.

[7] 47CFR15, Subpart B (Unintentional Radiators), U.S. Code of Federal Regulations, (formerly known as FCC Part 15, Subpart J).

[8] VDE 0871, Class "B", tested per VFG1046/1984.

[9] CISPR Publication 22, proposed new EC EMC Standard.

[10] Noise Reduction Techniques in Electronic Systems, 2nd ed., by Henry W. Ott, John Wiley & Sons, 1988.

[11] Protection of Electronic Circuits from Overvoltages, by Ronald B. Standler, John Wiley & Sons, 1989.

[12] Electromagnetic Compatibility for Industrial-Process Measurement and Control Equipment, Part 2: Electrostatic Discharge Requirements, IEC 801-2, 1991-04, draft.

[13] LONBUILDER NEURON C Programmer's Guide, by Echelon Corp., 1991.

[14] LONBUILDER User's Guide, by Echelon Corp., 1991.

[15] UL's LAN Cable Cerification Program. Document number 200-120 20M/11/91, by Underwriters Laboratories, Northbrook Illinios, (708) 272-8800

[16] Connector Wiring Guidelines for Typical LONWORKS Neytwork by Echelon Corp., 1992.

Suppliers

Socket Strips
Augat, Inc.
Methode Electronics Inc.
Samtec, Inc.
Samtec Electronics, LTD
32 Kbyte PLCC OTP ROMS
AMD (Advanced Micro Devices)
Atmel Inc.
Catalyst Semiconductor Inc.
Intel Corp.
Microchip Technology
National Semiconductor
Signetics Corp.
Texas Instruments, Inc.
PLCC/DIP Adapter
Emulation Technology, Inc.
Other
muRata-Erie

Appendix A

Application I/O Development Considerations

This appendix provides hints and suggestions to aid developers of application I/O hardware targeted for the Twisted Pair Control Modules. The I/O circuit designer is constrained by the programming model and internal hardware of the NEURON CHIP. The constraints on I/O pin usage are defined in References [1] and [13].

State Transition Timing

The state transition timing for NEURON CHIP I/O signals after reset depends on the external memory included in the node implementation. The Control Modules contain a fixed set of memory resources which do not include external RAM. Therefore, the I/O state transitions during reset are bounded by the slowest input clock frequency, 5 MHz. Figure A.1 shows typical I/O state transition behavior for a 5 MHz module during reset. The TP/XF-1250 modules running at 10 MHz will take roughly 61 ms to achieve the initial I/O pin state after the rising edge of the reset signal.

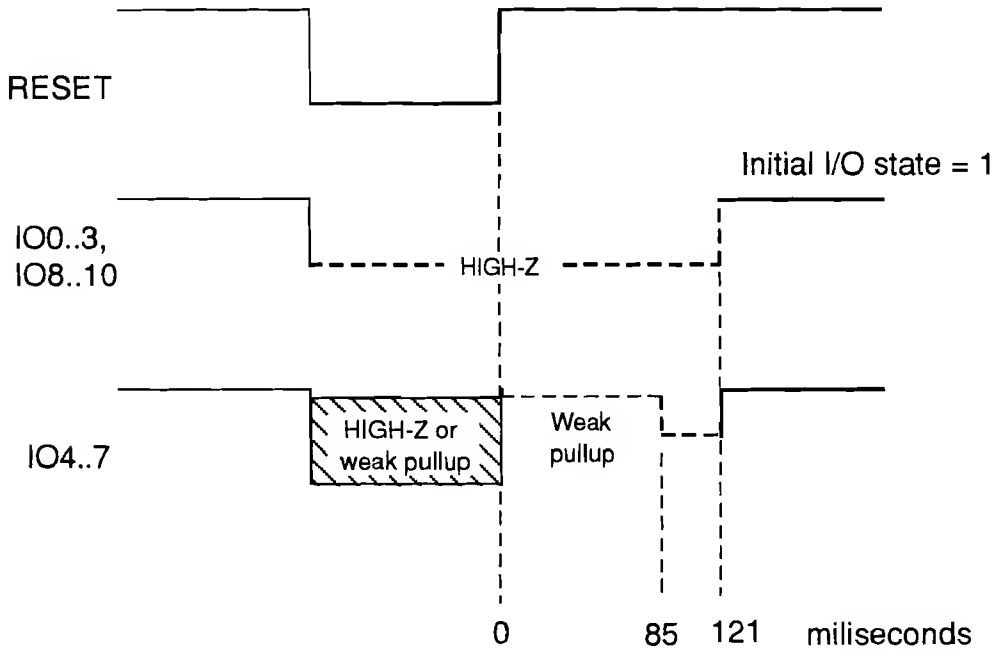

Figure A.1 Output pin state transitions for 5 MHz Control Modules

AIB Considerations

The LONBUILDER Developer's Workbench supports Twisted Pair Control Module I/O development with the following LONBUILDER accessories:

Application Interface Board (AIB), Model 27810

Module Application Interface, Model 21860

The AIB connects to the I/O expansion connector (P3) of a LONBUILDER Emulator or SBC. This board provides unbuffered access to the NEURON CHIP I/O signals through a front panel DB-25 connector. A shielded ribbon cable connects the AIB to the Module Application Interface which mates with a target application I/O board using the same header footprint as the Twisted Pair Control Module.

The model 21860 Module Application Interface board has two jumpers to control the power distribution for the I/O circuit under development. If JP1 is installed, the I/O circuit under development can use up to 400 mA of regulated +5V from the LONBUILDER through the pin P1.12. If JP2 is installed, 35 mA of regulated +12V from the LONBUILDER is available through pin P1.1. If the power supply circuit for the application I/O board sources the power, JP1 and JP2 must be removed.

The AIB does not buffer the 11-I/O and ~SERVICE pins of the NEURON CHIP. The ~SERVICE signal only reaches the interface adapter if the JP4 jumper marked on the AIB is installed.

The ~RESET signal on the AIB is a buffered CMOS input to the NEURON CHIP on the Emulator or SBC. This buffering does not allow direct testing of an I/O circuit using ~RESET as an output from the NEURON CHIP.

Appendix B

Example Power Supply

This appendix provides an example of a power supply with sufficient filtering to address RF noise levels.

Power Supply Circuit Example

The NEURON CHIP can generate significant levels of RF noise that must be suppressed to meet VDE and FCC regulations. The emission levels are significantly higher when the input clock to the NEURON CHIP is 10 MHz verses 5 MHz.

Left unchecked, the NEURON CHIP will generate significant levels of RF noise near 49 MHz through the external power supply input. The noise levels may be within FCC and VDE levels, but in the presence of RF LONWORKS transceivers, the RF media performance may be significantly impaired.

Figure B.1 shows an example power supply with sufficient filtering to address the issues described above.

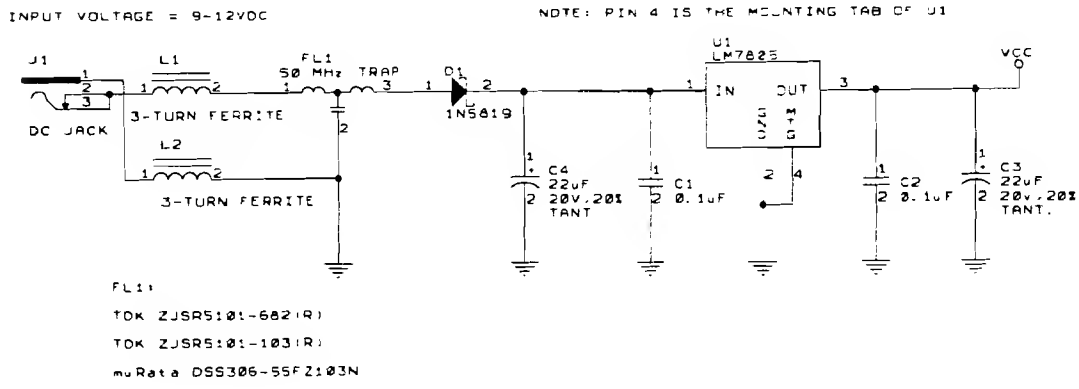

Figure B.1 Example Control Module power supply with EMI/RFI filters